Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

REMARKS

Claims 1-11, 14-16, 39 and 45-49 are currently pending. Claims 1 and 4 have been amended. The amendments to the claims are not made for reasons related to patentability. Rather, the amendments are provided for contextual purposes, and to add clarity. For example, although the recitations of depositing a conductive layer and planarizing the device were not in the claims as originally filed, these aspects are not narrowing because they further clarify what was already claimed, a process of forming a damascene structure.

Statement of the Substance of the Interview

On March 25, 2003, Thomas E. Lees, on behalf of the applicant, conducted a telephone interview with the Examiner. During the course of the interview, the application and Figures, particularly Figure 16, were discussed in detail in view of 35 U.S.C. §112, first paragraph, with respect to teaching a local interconnect and a gate in a damascene trench. In support thereof, the applicant directed the Examiner to several passages from the specification that describe local interconnects and gates in the same trench. The applicant also provided explanatory remarks in terms of distinguishing that which is shown in Fig. 16. Fig. 16 is a layout view of one exemplary use of the damascene structure of the present invention. The Examiner asserted that Fig. 16 was confusing in that he interpreted the Figure as showing interconnects and gates in separate trenches. The applicant agreed to modify Fig. 16 in a manner that does not introduce new matter that would clarify that Fig. 16 illustrates local interconnects and gates in the same trench. The nature of those changes is discussed in detail herein.

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

In the Specification

The specification has been amended herein to provide context, to add clarity, and to correct minor clerical matters. No new matter has been added. Specifically, the paragraph on page 11, starting at line 6 has been amended to clarify that the label identifying the gate conductor 72 is merely used to distinguish that portion of the conductive material within the damascene trench 44 that forms generally over the gate oxide 50 to point out where within the damascene trench that transistor gate structure is located. Likewise, the label of local interconnect conductor 74 is used merely to identify that portion of the damascene trench that defines a local interconnect to the substrate. This clarifies the teaching on page 9 starting at line 10 that each damascene trench can accommodate any number of interconnects and/or gates.

In The Drawings

The drawings were objected to under 37 C.F.R. §1.83(a). The Examiner asserts that the gate area and local interconnect area are not shown in the same trench as claimed in claims 1 and 39. This same objection was raised in the previous Office action. The applicant continues to rigorously assert that the drawings as originally filed, comply with 37 C.F.R. 1.83(a). However, in the spirit of cooperation with the Patent Office, the applicant respectfully submits herewith, a revised drawing sheet that includes clarifying changes to Fig. 16.

In amending Fig. 16, no new matter has been added. Rather, some changes were made to for contextual purposes and to add clarity. Referring to Fig. 16 as amended, the contacts 270, 272, 276 and 278 have been modified to be represented with dashed lines instead of solid lines as originally filed. The dashed lines are provided to further clarify that the contacts 270 and 272 are actually areas of the damascene trench 268 and not each separate trench structures distinct and apart from the damascene trench 268. Lik wise, contacts 276 and 278 are actually areas of the damascene trench 274. Support

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

for this change can be found in the specification for example, at page 15, lines 7-9, page 15, lines 14-17; page 15, lines 21-24; and page 15 starting at line 29 through page 16, line 2.

Note that in the formation of the damascene local interconnect according to an embodiment of the present invention, it is possible (though certainly not required) that there may be areas of gate oxide between a portion of the conductive material in the damascene trench and the substrate. This can result for example, due to masking, etching and other practical processing steps. As one example, while not limiting to the present invention, please initially refer to Fig. 4. Area 46 illustrates an exemplary portion of a damascene trench 46 where a local interconnect is to be built. As shown in Fig. 5, an oxide 50 is formed on the surface of the substrate 12. The oxide 50 will be later used to define the gate oxide portion of transistor gates in other portions of the substrate. Referring to Fig. 6, a third mask 60 is formed over the substrate, and a contact 62 to the substrate 12 is formed where the local interconnect structure is to be built. Note however, that as shown, small areas of oxide 50 still flank the contact 62. Referring now to Fig. 16, the contacts 270, 272, 276 and 278 are schematically illustrated with dashed circles slightly smaller than the adjacent strip of active area 294 to suggest that there may optionally be intermediate layers, such as the oxide 50 shown in Fig. 6 between the conductive material of the damascene trench and the substrate. The circles could have other dimensions of course. Also, the schematic representation of the contact as a circle is not intended to be limiting in any manner and the contact can take on any geometry.

Referring back to Fig. 16, each gate originally schematically represented with solid lines has been analogously replaced with dashed lines to clarify that the gates are portions of damascene trenches. Also, the size of the gates has been slightly enlarged to clarify again, that the gates define portions of damascene trenches. Particularly, gates 222 and 214 in damascene trench 268 have been amended to replace the solid box schematic

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

representation with dashed lines. Gates 238 and 230 in damascene trench 274 have likewise been amended to replace the solid box schematic representation with dashed lines. Likewise, the gates 248 and 258 in the damascene trench defining the wordline 255 (see top right of Fig. 16 and bottom left of Fig. 16) have been amended to replace the solid box schematic representation with dashed lines. Again, this change does not introduce new matter. Rather, the changes are presented for contextual purposes and to provide clarity. Support for the changes can be found in the specification for example, on page 15, lines 7-9; page 15, lines 15-17; page 15 lines 19-21; and page 15 lines 25-27.

The applicant asserts that, in view of the amendment to Fig. 16 and the clarifying remarks herein, the drawings are in compliance with 37 C.F.R. §1.83.

The applicant further respectfully traverses the Examiner's objection to claim 4 for not explicitly showing the steps in the formation of the isolation region. Claim 4 has been amended herein to merely recite etching into the base substrate defining an isolation trench opening in the base substrate and filling the isolation trench opening with a dielectric material. Fig. 1 shows this very structure as claim 4 is amended herein.

Moreover, 37 C.F.R. §1.83(a) states that conventional features disclosed in the description and claims should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box), where their detailed illustration is not essential for a proper understanding of the invention. The present application makes it clear that the manner in which the isolation trench is not essential to an understanding of the present invention. "The isolation trench 14 defines an isolation region, and is formed using any available techniques including for example, shallow trench isolation (STI) methods". Specification page 7, lines 12-14. Formation of the isolation regions as claimed is further explicitly described in the Specification on page 7 lines 25-29; pag 8, lin s 1-5. Moreover, trench formation is shown by a *rectangular box*

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

152 as suggested by 37 C.F.R. §1.83 in the flow chart of Fig. 14. The applicant asserts that, for all of the above reasons, the application is in compliance with 37 C.F.R. §1.83 for purposes of claim 4 as amended herein.

35 U.S.C. §112

Claims 1-11, 14-16, 39 and 45-49 were rejected under 35 U.S.C. §112 first paragraph. The Examiner asserts that the specification is not enabling for forming a gate structure and an interconnect structure in the same trench. The applicant respectfully traverses this rejection. The application makes clear that each damascene trench can actually include any combination of gates and local interconnects. Figs. 4-13 show the formation of both a gate and local interconnect. For purposes of clarity, a gate is formed in the damascene trench 44 (on the left hand side of the Figs.) and a local interconnect is shown in the damascene trench 46 (on the right hand side of the Figs). However, the specification makes clear that the damascene trenches are not limited to either a gate or an interconnect.

> "Further, any combination of gates and local interconnects can be formed within *each* of the gate/local interconnect damascene trenches 44, 46 as explained more fully herein" (emphasis added) Specification page 9, lines 10-12.

Also, one specific example is shown of using the techniques taught in the present invention to build an SRAM memory device as shown with reference to Figs. 15-16. As shown in Fig. 16, first and second strips 268, 274 (as well as word line 255) form conductive interconnects and may be fabricated as damascene trenches as discussed with reference to Figs. 1-13. Specification Page 15, lines 11-17.

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

The gates 214 and 222 are constructed as part of the first damascene trench 268 by building damascene gate structures. The first contact and second contact 270, 272 are constructed as part of the first damascene trench 268 by building damascene local interconnect structures. Likewise, the gates 224, 232 are constructed as part of the second damascene trench by building damascene gate structures. The third and fourth contacts 276, 278 are constructed as part of the second damascene trench by building damascene local interconnect structures. Specification Page 15, lines19-30.

The specification states that any combination of gates and local interconnects may be formed in a given damascene trench. Moreover, one exemplary structure discussed with reference to Figs. 15-16 illustrates two damascene trenches, each damascene trench having two local interconnect contacts and two gates formed therein. Fig. 16 has been amended herein to clarify that which was originally disclosed in the specification, that local interconnects and gates can be formed within a damascene trench.

Accordingly, the applicant asserts that the specification is enabling to one of ordinary skill in the art, and requests that the rejection with regard to 35 U.S.C. §112, first paragraph be withdrawn.

35 U.S.C. §103(a)

Claims 1, 5, 6, 8, 10, 46, 47 and 49 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 3,891,190 (Vadasz) in view of U.S. Patent No. 6,037,248 (Ahn). According to the M.P.E.P. §2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

With respect to claim 1 as amended herein, Vadasz combined with Ahn fails to teach or sugg st depositing a conductive layer over a base substrat such that a

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

damascene trench is filled with a conductive material and planarizing the device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by a conductive material within the damascene trench.

Discussion of Vadasz

As best seen in Figs. 1b and 1c of Vadasz, areas 14 are uncovered from a layer of oxide 12 previously built up on a semiconductor (Col. 3, lines 30-35). As seen in Fig. 1c, a thin oxide layer 20 is formed in the exposed areas 14. The device is masked, and a portion of the oxide 20 is removed from the area 14 defining an exposed area to the base substrate. A layer of silicon 24 is then formed over the structure (Fig. 1d, Col. 4, lines 1-12). Note however, that this is a conformal layer.

The applicant asserts that the area 14 is not a damascene trench. The specification in Vadasz is completely silent to characterizations that the area 14 is a damascene structure. Fig. 1d clearly shows a conformal layer of silicon that does not fill the area 14. Moreover, the specification of Vadasz does not teach or suggest planarizing the structure after depositing the silicon. For these and other reasons, it should be clear that a damascene structure is not taught by Vadasz.

Moreover, Vadasz arguably teaches away from the damascene process because Vadasz masks and removes all silicon from the area 14 except for the silicon that forms the gate, contacts and interconnects (Col. 4, lines 22-26). This structure is best seen in Figs. 1f and 2. As best seen in Fig. 2, the area 14 is not filled with a conductive material and there is no damascene trench and thus no damascene gate structure or damascene local interconnect structure electrically coupled by a conductive material.

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

Discussion of Ahn

Ahn does not teach damascene structures at all. Rather, vertically stacked interconnect structures are constructed by providing layers of photoresist material formed between conductive layers. The photoresist layers are subsequently removed leaving the conductive layers surrounded by air (Col. 3, lines 10-17). This structure is best seen in Figs. 9 and 10. While the air gaps 56 (Fig. 10) may provide a dielectric constant of 1, and while the structure may reduce plate capacitance, such structure neither teaches nor suggests what is claimed in claim 1 as amended herein. For example, as claimed, the gate and local interconnect are electrically coupled by a conductive material in the damascene trench. One feature of this structure is that it essentially eliminates gate to local interconnect contact resistance.

The specification and figures in Ahn merely show vias coupling conductive material to a substrate. The air gaps do not eliminate local interconnect to gate contact resistances at all. In fact, Ahn does not address local interconnect to gate contact resistance. For example, there are no illustrated connections to the gate 36. If there were, there would necessarily have to be contact resistance because the gate structure is formed prior to forming the vias for the interconnects (See Fig. 1; Col 4, lines 25-45).

The applicants assert that Vadasz combined with Ahn fails to teach or suggest all of the claimed limitations to claim 1 as amended herein. Accordingly, the applicant requests that the Examiner withdraw the rejection to claim 1, and the claims that depend therefrom, including claims 5, 6, 8, 10, 46, 47 and 49, under 35 U.S.C. §103

Claims 7, 9 and 11 were rejected under 35 U.S.C. §103 as being unpatentable over Vadasz in view of Ahn and the article Silicon Processing For The VLSI Era. Volume 2 – Process Integration by Lattice Press (hereinafter "Wolf").

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

Claims 7, 9 and 11 depend from claim 1, which has already been discussed with reference to Vadasz and Ahn above. Wolf does not teach or suggest the formation of damascene trenches at all. Further, Wolf does not teach or suggest the formation of interconnects. Accordingly, the applicant requests that the Examiner withdraw the rejection of claims 7, 9 and 11 under 35 U.S.C. §103.

Claims 1-3, 15, 45 and 48 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,083,827 (Lin) in view of Ahn.

Discussion of Lin

With respect to claim 1 as amended herein, Lin fails to teach or suggest forming a damascene trench in the first dielectric layer, the damascene trench having a gate area and a local interconnect area. As shown in Figs. 2A and 2B of Lin, transistor structures including the gates 204, 206, source drain regions 224, 226 and spacers 220, 222 are completely formed prior to forming a local interconnect structure (Col. 2, lines 53-65). The structure that the Examiner calls a damascene trench is merely an opening 232 (Col. 3, lines 8-12). The opening 232 is nothing more than a via that forms a local interconnect from the conductive layer 240 to a source/drain region 226.

Lin does not teach or suggest forming a gate oxide layer on the base substrate within said gate area of the damascene trench. As pointed out above, and as is shown in Fig. 2A-2B, the invention taught in Lin is an interconnect that is constructed during processing flow after transistor structures are formed. The applicant can find no mention in Lin whatsoever of a damascene trench.

Lin does not teach or suggest depositing a conductive layer over the base substrate and planarizing the device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

conductive material within said damascene trench. As pointed out above, in Lin, the gate structures are built first (Figs. 2A-2B, Col. 2, lines 57-61). Next an opening 232 is formed in the dielectric layer down to a source/drain region of the substrate (Fig. 2C; Col. 3, lines8-12). In a separate and subsequent process, a second opening 234 is formed which opens the gate poly silicon. Further, a cap layer 218 of the gate 206 is removed to transform the previously formed opening 232 into a local interconnect (Fig. 2D, Col. 3, lines13-17).

Further, as the Examiner points out, Lin does not teach or suggest removing the first dielectric layer. The Examiner relies upon Ahn for this teaching. However, there would be no motivation to combine Ahn and Lin. As is best demonstrated in Figs. 2A-2E of Lin, the structure taught in Lin is a two-step approach where transistor structures are constructed, then openings are created and cap layers over certain transistors are opened to form interconnects. After the interconnects are formed, a completed structure exists because the transistors had been previously formed. There is no need to remove the dielectric layer.

In the present invention, the dielectric layer is removed to allow further processing. For example, according to one embodiment of the invention, gate spacers and source drain regions are formed after removing the dielectric layer. In Lin however, the gates, source drain regions, and the entire transistor structure is completely built before even beginning to construct the interconnects.

Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 1 and the claims that depend therefrom, including claims 1-3, 15, 45 and 48 under 35 U.S.C. §103(a).

Received from < 937 223 0724 > at 4/25/03 3:08:33 PM [Eastern Daylight Time]

Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Lin in view of Wolf. As pointed out above, both Lin and Wolf fail to teach all of the limitations of claim 1, from which claim 4 depends. Accordingly, the applicant requests that the Examiner withdraw the rejection of claim 4 under 35 U.S.C. §103.

Allowable Subject Matter

The applicant would like to thank the Examiner for the indication of allowable subject matter of claims 14,16 and 39. The applicant believes that, based upon the amendments and remarks herein, the issues related to 35 U.S.C. §112, first paragraph have been addressed and these claims are now in condition for allowance.

CONCLUSION

For all of the above reasons, the applicant respectfully submits that the above claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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